FM20L08

1Mbit Bytewide FRAM Memory – Industrial Temp.

Features

1Mbit Ferroelectric Nonvolatile RAM
- Organized as 128Kx8
- Unlimited Read/Write Cycles
- NoDelay™ Writes
- Page Mode Operation to 33MHz
- Advanced High-Reliability Ferroelectric Process

SRAM Replacement
- JEDEC 128Kx8 SRAM pinout
- 60 ns Access Time, 350 ns Cycle Time

System Supervisor
- Low Voltage monitor drives external /LVL signal
- Write protects memory for low voltage condition

Superior to Battery-backed SRAM Modules
- No battery concerns
- Monolithic reliability
- True surface mount solution, no rework steps
- Superior for moisture, shock, and vibration
- Resistant to negative voltage undershoots

Low Power Operation
- 3.3V +10%, -5% Power Supply
- 22 mA Active Current

Industry Standard Configurations
- Industrial Temperature -40° C to +85° C
- 32-pin "Green"/RoHS TSOP (-TG)

Description

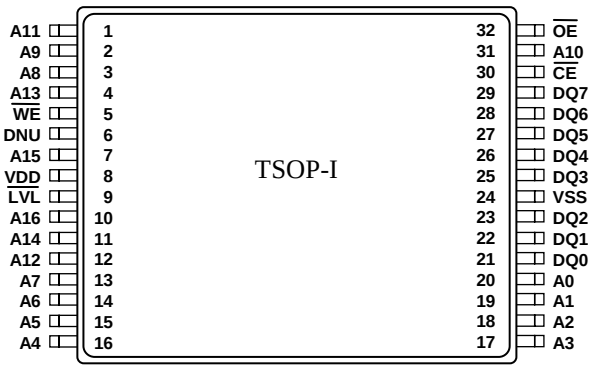
The FM20L08 is a 128K x 8 nonvolatile memory that reads and writes like a standard SRAM. A ferroelectric random access memory or FRAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 10 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and unlimited write endurance make FRAM superior to other types of memory.

In-system operation of the FM20L08 is very similar to other RAM devices and can be used as a drop-in replacement for standard SRAM. Read and write cycles may be triggered by /CE or simply by changing the address. The FRAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM20L08 ideal for nonvolatile memory applications requiring frequent or rapid writes in the form of an SRAM.

The FM20L08 includes a voltage monitor function that monitors the power supply voltage. It asserts an active-low signal that indicates the memory is write-protected when V_{DD} drops below a critical threshold. When the /LVL signal is low, the memory is protected against an inadvertent access and data corruption.

Device specifications are guaranteed over the industrial temperature range -40°C to +85°C.

Pin Configuration



Ordering Information	
FM20L08-60-TG	60 ns access, 32-pin "Green"/RoHS TSOP

Ramtron International Corporation
1850 Ramtron Drive, Colorado Springs, CO 80921
(800) 545-FRAM, (719) 481-7000

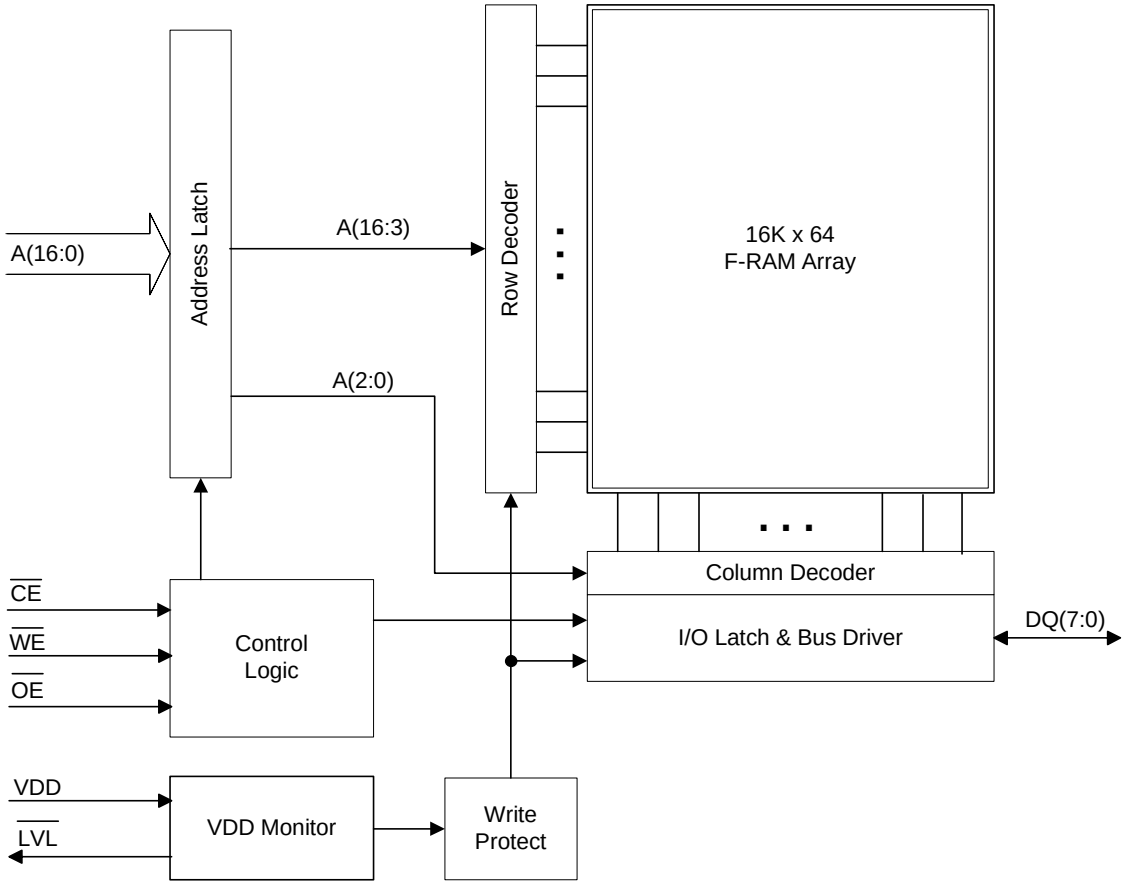


Figure 1. Block Diagram

Pin Description

Pin Name	Type	Pin Description
A(16:0)	Input	Address inputs: The 17 address lines select one of 131,072 bytes in the FRAM array. The address value is latched on the falling edge of /CE. Addresses A(2:0) are used for page mode read and write operations.
/CE	Input	Chip Enable inputs: The device is selected and a new memory access begins when /CE is low. The entire address is latched internally on the falling edge of chip enable. Subsequent changes to the A(2:0) address inputs allow page mode operation.
/WE	Input	Write Enable: A write cycle begins when /WE is asserted. The rising edge causes the FM20L08 to write the data on the DQ bus to the FRAM array. The falling edge of /WE latches a new column address for fast page mode write cycles.
/OE	Input	Output Enable: When /OE is low, the FM20L08 drives the data bus when valid data is available. Deasserting /OE high tri-states the DQ pins.
DQ(7:0)	I/O	Data: 8-bit bi-directional data bus for accessing the FRAM array.
/LVL	Output	Low Voltage Lockout: When the voltage monitor detects that V_{DD} is below V_{TP}, the /LVL pin will be asserted low. While /LVL is low, the memory array cannot be accessed which prevents a low voltage write from corrupting data. When V_{DD} is within its normal operating limits, the /LVL signal will be pulled high.
DNU	-	Do Not Use: This pin should be left unconnected.
VDD	Supply	Supply Voltage: 3.3V
VSS	Supply	Ground

Functional Truth Table

/CE	/WE	A(16:3)	A(2:0)	Operation
H	X	X	X	Standby/Idle
↓	H	V	V	Read
L	H	No Change	Change	Page Mode Read
L	H	Change	V	Random Read
↓	L	V	V	/CE-Controlled Write
L	↓	X	V	/WE-Controlled Write [2]
L	↓	No Change	V	Page Mode Write [3]
↑	X	X	X	Starts Precharge

Notes:

1) H=Logic High, L=Logic Low, V=Valid Address, X=Don't Care.
2) /WE-controlled write cycle begins as a Read cycle and A(16:3) is latched then.
3) Addresses A(2:0) must remain stable for at least 15 ns during page mode operation.
4) For write cycles, data-in is latched on the rising edge of /CE or /WE, whichever comes first.

Overview

The FM20L08 is a bytewide FRAM memory logically organized as 131,072 x 8 and is accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation which provides higher speed access to addresses within a page (row). An access to a different page requires that either /CE transitions low or the upper address A(16:3) changes.

Memory Operation

Users access 131,072 memory locations with 8 data bits each through a parallel interface. The FRAM array is internally organized as 16K rows of 64 bits each. Within each row (page) there are 8 column locations, which allow fast access in page mode operation. Once an initial address has been latched by the falling edge of /CE, subsequent column locations may be accessed without the need to toggle /CE. When /CE is deasserted high, a precharge operation begins. Writes occur immediately at the end of the access with no delay. The /WE pin must be toggled for each write operation.

Read Operation

A read operation begins on the falling edge of /CE. The falling edge of /CE causes the address to be latched and starts a memory read cycle if /WE is high. Data becomes available on the bus after the access time has been satisfied. Once the address has been latched and the access completed, a new access to a random location (different row) may begin while /CE is still low. The minimum cycle time for random addresses is t_{RC}. Note that unlike SRAMs, the FM20L08's /CE-initiated access time is faster than the address cycle time.

The FM20L08 will drive the data bus only when /OE is asserted low and the memory access time has been satisfied. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is inactive, the data bus will remain hi-Z.

Write Operation

Writes occur in the FM20L08 in the same time interval as reads. The FM20L08 supports both /CE- and /WE-controlled write cycles. In both cases, the address is latched on the falling edge of /CE.

In a /CE-controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the device begins the memory cycle as a write. The FM20L08 will not drive the data bus regardless of the state of /OE as long as /WE is low. Input data must be valid when /CE is deasserted high. In a /WE-controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if /OE is low, however it will hi-Z once /WE is asserted low. The /CE- and /WE-controlled write timing cases are shown on page 9. In the *Write Cycle Timing 2* diagram, the data bus is shown as a hi-Z condition while the chip is write-enabled and before the required setup time. Although this is drawn to look like a mid-level voltage, it is recommended that all DQ pins comply with the minimum V_{IH}/V_{IL} operating levels.

Write access to the array begins on the falling edge of /WE after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever comes first. A valid write operation requires the user to meet the access time specification prior to deasserting /WE or /CE. Data setup time indicates the interval during which data cannot change prior to the end of the write access (/WE or /CE high).

Unlike other nonvolatile memory technologies, there is no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Page Mode Operation

The FM20L08 provides the user fast access to any data within a row element. Each row has eight column locations. An access can start anywhere within a row and other column locations may be accessed without the need to toggle the /CE pin. For page mode reads, once the first data byte is driven onto the bus, the column address inputs A(2:0) may be changed to a new value. A new data byte is then driven to the DQ pins. For page mode writes, the first write pulse defines the first write access. While /CE is low, a subsequent write pulse along with a new column address provides a page mode write access.

Precharge Operation

The precharge operation is an internal condition in which the state of the memory is prepared for a new access. Precharge is user-initiated by driving the /CE signal high. It must remain high for at least the minimum precharge time t_{PC}.

Supply Voltage Monitor

An internal voltage monitor circuit continuously checks the V_{DD} supply voltage. When V_{DD} is below the specified threshold V_{TP}, the monitor asserts the /LVL signal to an active-low state. The FM20L08 locks out access to the memory when V_{DD} is below the trip voltage. This prevents the system from accessing memory when V_{DD} is too low and inadvertently corrupting the data. The /LVL signal should not be used as a system reset signal because the system host may attempt to write data to the FM20L08 below its specified operating voltage. The /LVL pin may be used as a status indicator that the memory is locked out.

On power up, the /LVL signal will begin in a low state signifying that V_{DD} is below the V_{TP} threshold. It will remain low as long as V_{DD} is below that level. Once V_{DD} rises above V_{TP}, a hold-off timer will begin creating the delay t_{PULV}. Once this delay has elapsed, the /LVL signal will go high or inactive. At this time the memory can be accessed. The memory is ready for access prior to t_{PU} as shown in the Electrical Specifications section. The /LVL signal will remain high until V_{DD} drops below the threshold.

SRAM Drop-In Replacement

The FM20L08 has been designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require /CE to toggle for each new address. /CE may remain low indefinitely while V_{DD} is applied. When /CE is low, the device automatically detects address changes and a new access is begun. It also allows page mode operation at speeds up to 33MHz.

Although /CE may be held low for extended periods of time, the pin should not be tied to ground or held low during power cycles. /CE must be pulled high and allowed to track V_{DD} during powerup and powerdown cycles. It is the user's responsibility to ensure that chip enable is high to prevent incorrect operation. Figure 2 shows a pullup resistor on /CE which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /CE pin tracks V_{DD} yet a high enough value that the current drawn when /CE is low is not an issue.

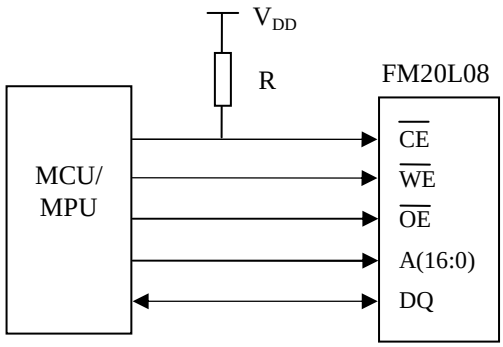


Figure 2. Use of Pullup Resistor on /CE

For applications that require the lowest power consumption, the /CE signal should be active only during memory accesses. Due to the external pullup resistor, some supply current will be drawn while /CE is low. When /CE is high, the device draws no more than the maximum standby current I_{SB}.

The FM20L08 is backward compatible with the 256Kbit FM18L08 device. So, operating the FM20L08 with /CE toggling low on every address is perfectly acceptable.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +5.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +5.0V and $V_{IN} < V_{DD}+1V$
T_{STG}	Storage Temperature	-55°C to +125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	300° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Charged Device Model (JEDEC Std JESD22-C101-A) - Machine Model (JEDEC Std JESD22-A115-A)	 3kV 750V 200V
	Package Moisture Sensitivity Level	MSL-2

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to +85° C, V_{DD} = 3.3V +10%, -5% unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	3.135	3.3	3.63	V	
I_{DD}	V_{DD} Supply Current		-	22	mA	1
I_{SB}	Standby Current – CMOS		-	25	µA	2
V_{TP}	V_{DD} trip point to assert (deassert) /LVL	2.7	-	3.0	V	3
I_{LI}	Input Leakage Current			±1	µA	4
I_{LO}	Output Leakage Current			±1	µA	4
V_{IH}	Input High Voltage	2.2		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.6	V	
V_{OH}	Output High Voltage (I_{OH} = -1.0 mA)	2.4		-	V	
V_{OL}	Output Low Voltage (I_{OL} = 2.1 mA)	-		0.4	V	5

Notes

1. V_{DD} = 3.6V, /CE cycling at minimum cycle time. All inputs at CMOS levels (0.2V or V_{DD}-0.2V), all DQ pins unloaded.
2. V_{DD} = 3.6V, /CE at V_{DD}, All other pins at CMOS levels (0.2V or V_{DD}-0.2V).
3. This is the V_{DD} trip voltage at which /LVL is asserted or deasserted. When V_{DD} rises above V_{TP}, /LVL will be deasserted after satisfying t_{PULV}. When V_{DD} drops below V_{TP}, /LVL will be asserted after satisfying t_{PDLV}.
4. V_{IN}, V_{OUT} between V_{DD} and V_{SS}.
5. For the /LVL pin, the test condition is I_{OL} = 80 µA when V_{DD} is between 3.135V and 1.2V. The state of the /LVL pin is not guaranteed when V_{DD} is below 1.2V.

Read Cycle AC Parameters (T_A = -40° C to +85° C, C_L = 30 pF, V_{DD} = 3.3V +10%, -5% unless otherwise specified)

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{RC}	Read Cycle Time	350	-	ns	
t_{CE}	Chip Enable Access Time	-	60	ns	
t_{AA}	Address Access Time	-	350	ns	
t_{OH}	Output Hold Time	50	-	ns	
t_{AAP}	Page Mode Address Access Time	-	25	ns	
t_{OHP}	Page Mode Output Hold Time	5	-	ns	
t_{CA}	Chip Enable Active Time	60	-	ns	
t_{PC}	Precharge Time	290	-	ns	
t_{AS}	Address Setup Time (to /CE low)	5	-	ns	
t_{AH}	Address Hold Time (/CE-controlled)	60	-	ns	
t_{OE}	Output Enable Access Time	-	10	ns	
t_{HZ}	Chip Enable to Output High-Z	-	15	ns	1
t_{OHZ}	Output Enable High to Output High-Z	-	15	ns	1

Write Cycle AC Parameters (T_A = -40° C to +85° C, V_{DD} = 3.3V +10%, -5% unless otherwise specified)

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{WC}	Write Cycle Time	350	-	ns	
t_{CA}	Chip Enable Active Time	60	-	ns	
t_{CW}	Chip Enable to Write Enable High	60	-	ns	
t_{PC}	Precharge Time	290	-	ns	
t_{PWC}	Page Mode Write Enable Cycle Time	30	-	ns	
t_{WP}	Write Enable Pulse Width	15	-	ns	
t_{AS}	Address Setup Time (to /CE low)	5	-	ns	
t_{AH}	Address Hold Time (/CE-controlled)	60	-	ns	
t_{ASP}	Page Mode Address Setup Time (to /WE low)	5	-	ns	
t_{AHP}	Page Mode Address Hold Time (to /WE low)	15	-	ns	
t_{WLC}	Write Enable Low to /CE High	25	-	ns	
t_{WLA}	Write Enable Low to A(16:3) Change	25	-	ns	
t_{AWH}	A(16:3) Change to Write Enable High	350	-	ns	
t_{DS}	Data Input Setup Time	20	-	ns	
t_{DH}	Data Input Hold Time	0	-	ns	
t_{WZ}	Write Enable Low to Output High Z	-	15	ns	1
t_{WX}	Write Enable High to Output Driven	5	-	ns	1
t_{WS}	Write Enable to /CE Low Setup Time	0	-	ns	1,2
t_{WH}	Write Enable to /CE High Hold Time	0	-	ns	1,2

Notes

1 This parameter is characterized but not 100% tested.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs.

Power Cycle Timing (T_A = -40° C to +85° C, V_{DD} = 3.3V +10%, -5% unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{PULV}	Power Up to /LVL Inactive Time (V_{TP} to /LVL high)	0	5	ms	
t_{PDLV}	Power Down to /LVL Active Time (V_{TP} to /LVL low)	0	15	µs	
t_{PU}	Power Up (/LVL high) to First Access Time	0	-	µs	
t_{PD}	Last Access (/CE high) to Power Down (V_{DD} min)	0	-	µs	
t_{VR}	V_{DD} Rise Time	50	-	µs/V	1
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1

Notes

1 Slope measured at any point on V_{DD} waveform.

Data Retention (V_{DD} = 3.3V +10%, -5%)

Parameter	Min	Max	Units	Notes
Data Retention	10	-	Years	

Capacitance (T_A = 25° C , f=1 MHz, V_{DD} = 3.3V)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (DQ)	-	8	pF	1
C_{IN}	Input Capacitance	-	6	pF	1

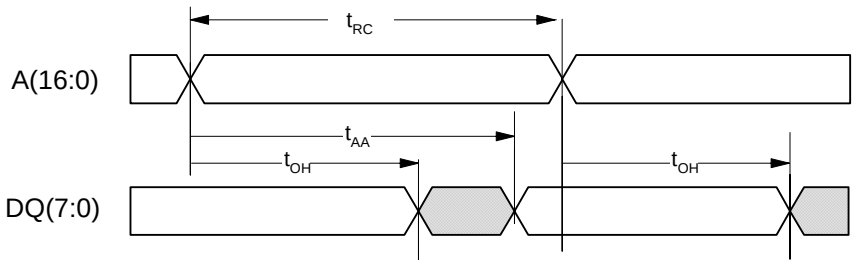
Notes

1. This parameter is characterized and not 100% tested.

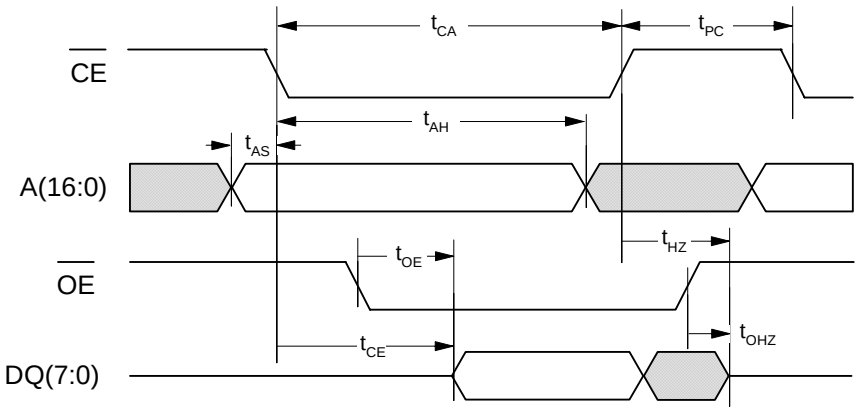
AC Test Conditions

Input Pulse Levels	0 to 3V
Input rise and fall times	3 ns
Input and output timing levels	1.5V
Output Load Capacitance	30 pF

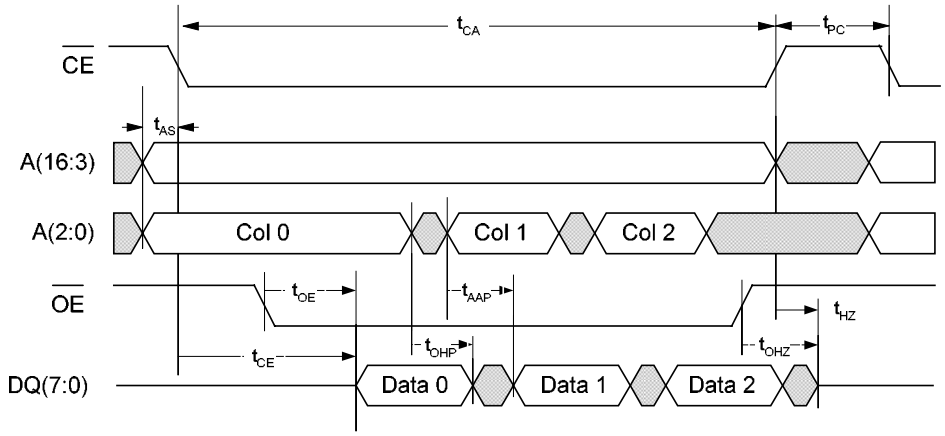
Read Cycle Timing 1 (/CE low, /OE low)



Read Cycle Timing 2 (/CE-controlled)

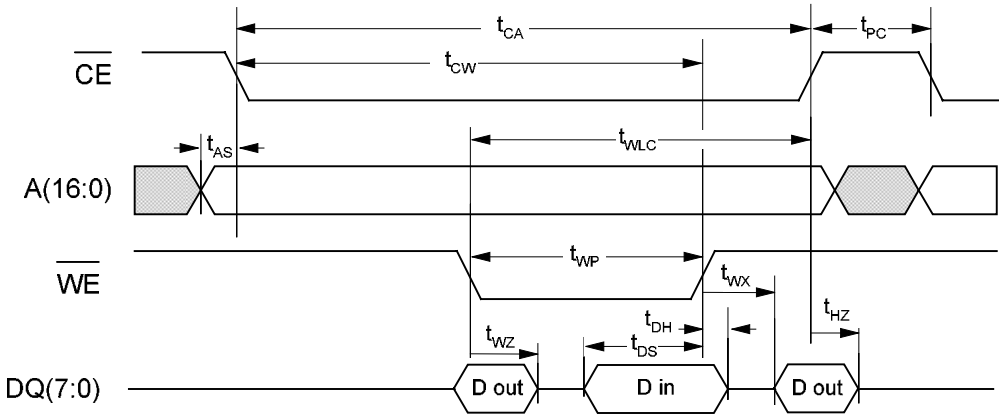


Page Mode Read Cycle Timing

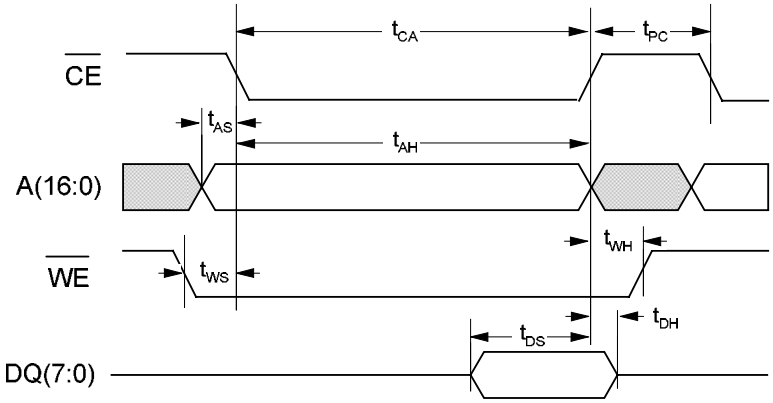


Although sequential column addressing is shown, it is not required.

Write Cycle Timing 1 (/WE-Controlled, /OE low)

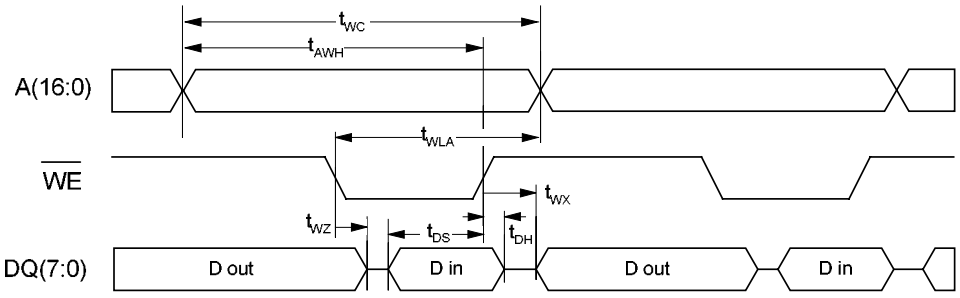


Write Cycle Timing 2 (/CE-Controlled)

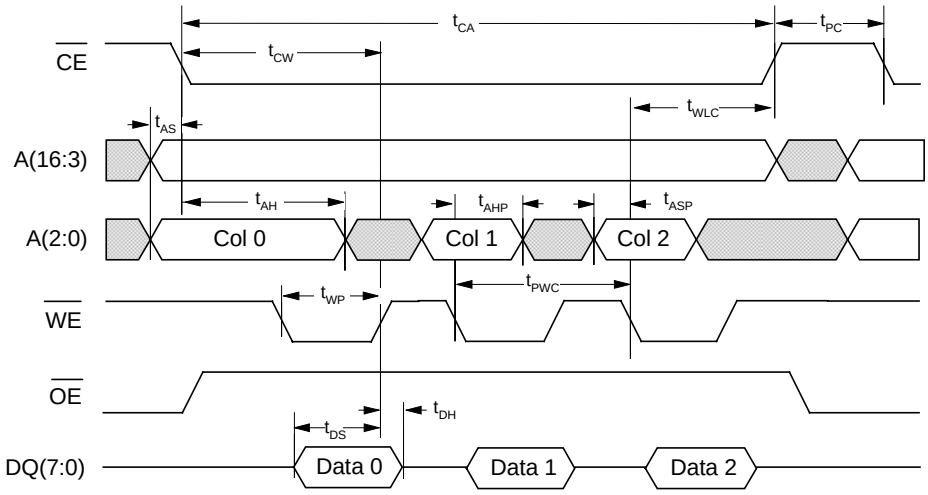


NOTE: See Write Operation section for detailed description (page 4).

Write Cycle Timing 3 (/CE low)

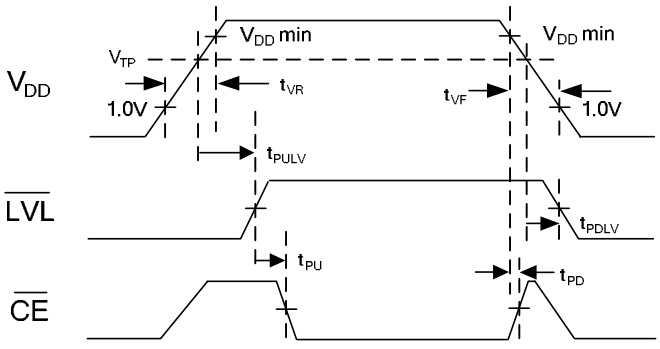


Page Mode Write Cycle Timing



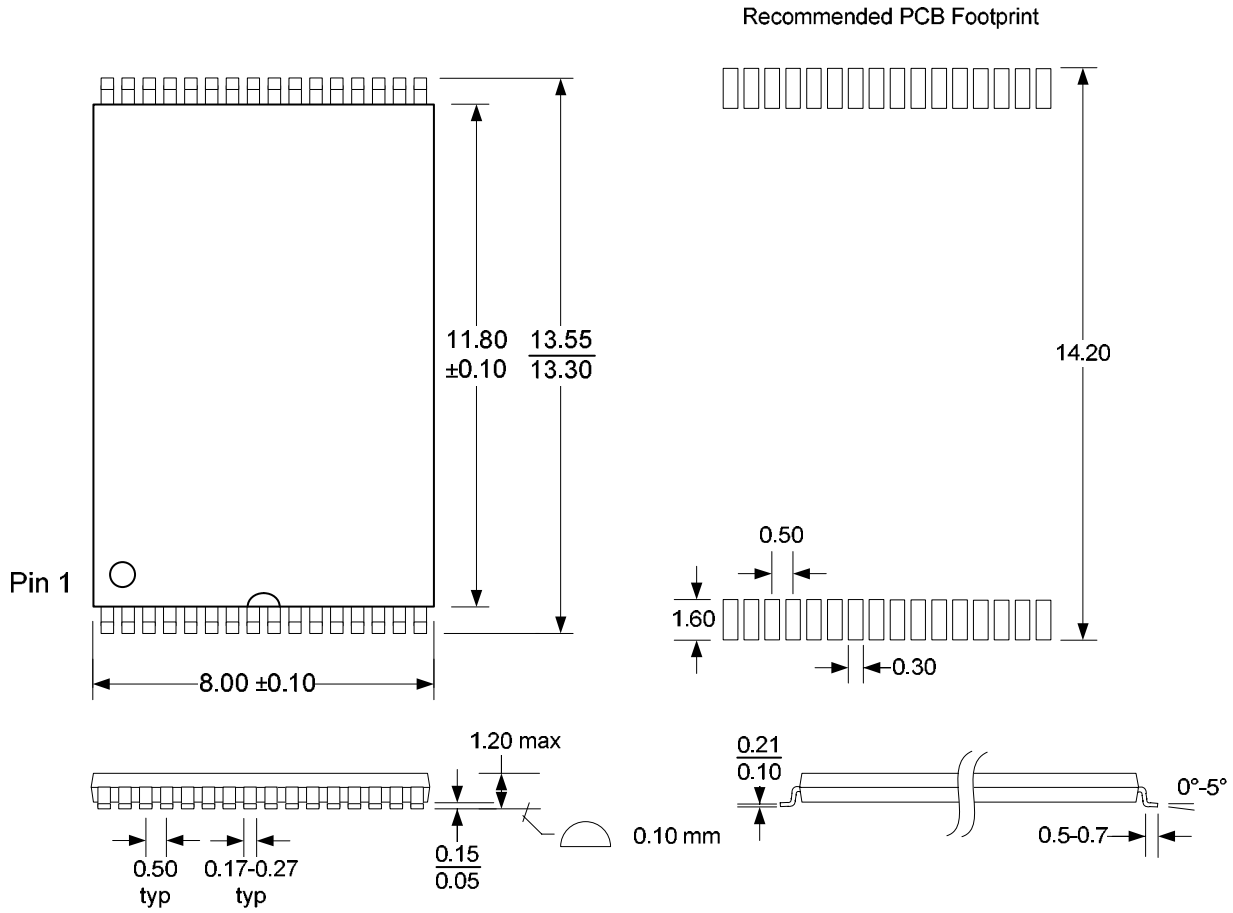
Although sequential column addressing is shown, it is not required.

Power Cycle Timing

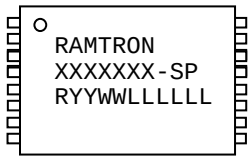


Mechanical Drawing

32-pin Shrunk TSOP-I (8.0 x 13.4 mm)
All dimensions in millimeters



TSOP Package Marking Scheme



Legend:
XXXXXX= part number, SP= speed/package/temp (blank=ind., C=extended)
R=rev code, YY=year, WW=work week, LLLLLL= lot code

Examples: "Green" TSOP package, Industrial temp,
B rev., Year 2006, Work Week 44, Lot 60011TG

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RAMTRON
FM20L08-60TG
B064460011TG
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Revision History

Revision	Date	Summary
0.6	1/30/04	Added Vdd fall time spec. Changed Power Cycle Timing diagram. Added t_{AWH} Write Timing spec. Added typ value to V_{TP} in DC Operating table. Changed software write-protect scheme. Changed /LVL to Output-only pin. Modified Block Diagram, Pin Description and DC Operating tables. Modified package drawing title.
0.61	5/20/04	Changed t_{WX}, t_{AAP}, and t_{AWH} specs. Added t_{AH} to Write Cycle parameters table. Changed input rise/fall time AC test condition. Changed t_{VF} units. Added "green" package.
0.7	9/3/04	Reduced to one speed grade and changed to -60 speed grade. Supply voltage 3.3V +10%, -5%. Temp range 0 to +85C.
0.8	12/20/04	Temp range -40 to +85C. Changed AC timing parameters. Changed part number/ordering information.
1.0	3/25/05	Changed to Preliminary status.
1.1	5/23/05	Added "green" packaging option. Added marking scheme.
1.2	6/6/05	Removed –T packaging option.
1.3	8/15/05	Changed address setup and I_{DD} specs. Added t_{VR} parameter. Added note about /CE high during power cycles. Modified Power Cycle timing diagram and added timing parameters. Removed references to the use of /LVL as a system reset signal. Changed temperature limits.
1.4	10/18/05	Changed I_{SB}. Changed V_{TP} limits. Added note to Power Cycle Timing table. Rewrote text describing use of pullup resistor.
1.5	2/9/06	Order device with or without software WP. Changed t_{PULV} to 5ms. Added ESD and MSL ratings.
1.6	6/12/06	Changed specs to industrial temperature. Devices with date codes 0605 through 0620 comply with this datasheet revision.
1.7	8/21/06	Changed I_{SB} spec. Updated ESD ratings. Removed Note 2 from Power Cycle Timing table. Devices with date codes 0624 and beyond comply with this datasheet revision.
1.71	4/9/07	Changed Package Marking Scheme. Updated ESD machine model and MSL ratings.
1.72	5/10/07	Added pcb footprint to package drawing.
1.8	5/6/2008	Removed –TG1 (software write protect) ordering number.